What is claimed is:

1. A processing system comprising:

a memory controller adapted to issue and receive commands in a packet based protocol;

a cache memory;

a plurality of memory modules comprising SDRAM devices; and

a single interface device located with the memory controller such that the interface device is not located on the memory modules, the interface device adapted to translate packet based protocol command and data signals from the memory controller into an SDRAM protocol, and the interface device adapted to translate data signals received from the memory module into packet based protocol data.

2. The processing system of claim 1 wherein the memory controller is provided in an integrated circuit chip set.

3. The processing system of claim 2 wherein the integrated circuit chip set comprises the single interface device.

4. The processing system of claim 1 wherein the memory controller and single interface device are provided on a motherboard.

5. A processing system comprising:

a memory controller adapted to issue and receive commands in a packet based protocol;

a cache memory;

a plurality of memory modules comprising SDRAM devices, the plurality of memory modules each being located in a memory socket; and

a single interface device located between the memory controller and the memory sockets, the interface device adapted to translate packet based protocol command and data signals from the memory controller into an SDRAM protocol, and the interface device adapted to translate data signals received from the memory module into packet based protocol data.

6. The processing system of claim 5 wherein the memory controller and single interface device are provided on a motherboard.

7. The processing system of claim 5, wherein the single interface device supports either matched or unmatched data input and output bandwidth.

8. The processing system of claim 5 wherein the single interface device comprises:

a write demultiplex circuit adapted to convert data received on N data lines from the memory controller to M x N data lines;

a read multiplex circuit adapted to convert received data on the M x N data lines from the memory module to the N data lines; and

a command disassembler adapted to convert packet based commands from the memory controller into row/column based commands.

9. A processing system comprising:

a memory controller adapted to issue and receive commands in a packet based protocol;

a cache memory;

a plurality of memory modules comprising SDRAM devices, the plurality of memory modules each being located in a memory socket; and

a single interface device located between the memory controller and the memory sockets, the interface device adapted to translate packet based protocol command and

data signals from the memory controller into an SDRAM protocol, the interface device comprises:

a write demultiplex circuit adapted to convert data received on N data lines from the memory controller to M x N data lines;

a read multiplex circuit adapted to convert received data on the M x N data lines from the memory module to the N data lines; and

a command disassembler adapted to convert packet based commands from the memory controller into row/column based commands.

10. The processing system of claim 9, wherein the memory controller and single interface device are provided on a motherboard.

11. The processing system of claim 9, wherein the single interface device supports either matched or unmatched data input and output bandwidth.

12. The processing system of claim 9, wherein the memory controller is provided in an integrated circuit chip set.

13. The processing system of claim 12, wherein the integrated circuit chip set comprises the single interface device.

14. A processing system comprising:

a memory controller adapted to issue and receive commands in a packet based protocol;

a cache memory;

a plurality of memory modules each comprising column/row protocol based devices, the memory modules are located in in-line memory module sockets; and

a single interface device located between the memory controller and the in-line memory module sockets, the interface device adapted to translate packet based protocol

command and data signals from the memory controller into the column/row protocol, and the interface device adapted to translate data signals received from the memory modules into packet based protocol data.

15. The processing system of claim 14, wherein the memory controller is provided in an integrated circuit chip set.

16. The processing system of claim 15, wherein the integrated circuit chip set comprises the single interface device.

17. The processing system of claim 14, wherein the memory controller and single interface device are provided on a motherboard.

18. A processing system motherboard comprising:

a memory controller adapted to issue and receive commands in a packet based protocol;

a cache memory; and

a single interface device adapted to translate packet based protocol command and data signals from the memory controller into a column/row protocol, and adapted to translate data signals received from the plurality of memory modules that are located external to the motherboard into the packet based protocol data.

19. The processing system motherboard of claim 18, further comprising a processor.

20. The processing system motherboard of claim 18, wherein the column/row protocol is a synchronous dynamic random access memory column/row protocol.

21. A processing system comprising:

a processor; and

a chip set, comprising:

a memory controller adapted to issue and receive commands in a packet based protocol;

a cache memory coupled to the processor, and

a single interface device adapted to translate packet based protocol command and data signals from the memory controller into a column/row protocol, and adapted to translate data signals received from the plurality of memory modules, each of the memory modules being separately detachable from the interface device into the packet based protocol data.

22. The processing system chip set of claim 21, wherein the single interface device comprises:

a write demultiplex circuit adapted to convert data received on N data lines from the memory controller to M x N data lines;

a read multiplex circuit adapted to convert received data on the M x N data lines from an external memory to the N data lines; and

a command disassembler adapted to convert packet based commands from the memory controller into the row/column commands.

23. A processing system comprising:

a processor;

a cache memory coupled to the processor;

a plurality of memory modules comprising SDRAM devices, the plurality of memory modules each being located in a memory socket;

a chip set, comprising:

a memory controller adapted to issue and receive commands in a packet based protocol; and

a single interface device located between the memory controller and the memory sockets, the interface device adapted to translate packet based protocol command and data signals from the memory controller into an SDRAM protocol.

24. The processing system of claim 23 wherein the memory controller and single interface device are provided on a motherboard.